a first data line extending along said first direction and coupled commonly to said first and second internal data lines in said first and second amplifier blocks while being isolated from said third internal data line in said third amplifier block, said first and second amplifier blocks thereby being coupled to a common first input-output circuit via said first data line independently from said third amplifier block;

a second data line extending along said first direction and coupled to said third internal data [lines] line in said third amplifier block and thereby coupling said third amplifier block to a second input-output circuit independently from said first and second amplifier blocks.

4. A semiconductor memory device comprising:

a plurality of memory cell blocks each including a first and a second group of memory cells, said memory cell blocks being arranged in a first direction;

a first amplifier block provided adjacently to one end of an arrangement of said memory cell blocks, coupled to one of said first and second groups in one of said memory cell blocks on said one end, and selectively transferring a data of one of said memory cells in said one of said first and second groups via a first internal data line extending in a second direction different from said first direction;

a second amplifier block provided adjacently to another end of said arrangement, coupled to one of said first and second groups in one of said memory cell blocks on said another end, and selectively transferring a data of one of said memory cells in said one of first and second groups via a second internal data line thereof extending in said second direction;

at least one third amplifier block arranged between said memory cell blocks, coupled to one of said first and second groups in one of said memory cell blocks adjacent to one side thereof, and to one of said first and second groups in one of said memory cell blocks adjacent to another side thereof, and selectively transferring a data of one of said groups coupled thereto via a third internal data line thereof extending along said second direction;

a first data line extending along said first direction and coupled commonly to said first and second internal data lines in said first and second amplifier blocks while being isolated from said third internal data line in said third amplifier block; and

a second data line extending along said first direction and coupled to said third internal data line in said third amplifier block.

9. A semiconductor memory device as claimed in claim 8, further comprising:

a plurality of sense amplifiers in each of said first, second and third amplifier blocks, each of said sense amplifiers having a pair of input nodes; and

a plurality of pairs of parallel bit lines extending in said columns, one and another of bit lines in one of said pairs of bit lines providing a reference potential and a read signal to be applied to said sense amplifier, said sense amplifier in said third amplifier block having said pair of input nodes thereof operatively connected to either one of said pairs of bit lines in one of said memory cell blocks facing to one side of said third amplifier block and another pair of bit lines in another memory cell block facing to another side of said third amplifier block.

15. A semiconductor memory device as claimed in claim 12, wherein each of said memory cell blocks includes said memory cells arranged in rows and columns, said columns extending in said first direction, one of said first and second memory cells belonging to an even numbered column, another of said first and second memory cells belonging to an odd numbered column.

20. A combination as claimed in claim 19, further comprising:

for each of said amplifier blocks, a respective signal line, extending in a second direction perpendicular to said first direction, for transferring a data signal from an associated one of said memory cell blocks;

said first data line being coupled, at a first side thereof, to said respective signal line of said first amplifier block;

said first data line being coupled, at a second side thereof, to said respective signal line of said last amplifier block.

REMARKS

General remarks:

Claims 1-20 are all the claims pending in the application. Claims 1, 3, 12, 13/12, 14/13/12, and 19 are allowed.